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DESIGN AND IMPLEMENTATION OF A MULTIPLE-VALUED LOGIC FPGA BASED ON CONVERT–CODED-COLLECT (CCCI) SPACE THEORY

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ABSTRACT

The Multiple-Valued Logic (MVL) is one of the keys to build the future logic circuits. One of the most important logic units is Field Programming Gate Array (FPGA). Multiple-valued FPGA structures have interconnections less than that in binary FPGAs. Because the inherent dominate delay, power and size the Multiple-valued logic offers overcoming such issues, such as reduction of the number of signals in the circuit.

This Works proposes a new structure of FPGA that based on a new theory of multiple-valued logic (MVL) called Convert-Coded-Collectspace (CCCi). The CCC is paceis a closed space with iinteger values, used to convert the input to output in three phases called convert phase, coded phase, and collect phase, respectively. This paper implement a quaternary FPGA also, it show an example to design a logic multiplexer and flip-flop, under CCC4 space to verify of the new theory for MVL where the two examples are the basic elements of FPGA cells.

KEYWORDS: Multiple Valued Logic, Interconnections, FPGA, CCCi Space, Multiplexer, Flip-Flop

I. INTRODUCTION

Field Programming Gate Array (FPGA) structures are widely used due to early time-to-market and reduced non-recurring engineering costs in comparison to Application Specific Integrated Circuits (ASIC) designs. Interconnections playa crucial role in modern FPGAs, because they dominatedelay, power and size. Multiple-valued logic has received increased attention in the last decades because of the possibility to represent the information with more than two discrete levels. Representing data using an MVL system is more effective than the binary-based representation, because the number of interconnections can be significantly reduced, with major impact in all design parameters: less area interconnections; more compact and shorter interconnections, leading to increased performance; lower interconnect switched capacitance, and hence lower global power dissipation [1]. Multiple-valued logic (MVL) allows the reduction of the number of signals in the circuit, hence may serve as a mean to effectively curtail the impact of interconnections [2], [3]. There are two main interconnection problem faced the present binary logic systems, both on-chip and between chips. With the increasingcapability per chip, the difficulties of placement and routing, on chip, of the digital logicelements are escalating [4], [5]. Because of the advantages of multiple-valued logic, it has been used in several important fields like communication, digital signal processing [6]. The proposed work in thispaper deals with the use of a new theory called Convert-Coded-Collect (CCCi) space for implementing a new Multi-Valued Logic FPGA. This work presents an extension the binary logic to MVL and verifying the new theory by designing new combinational and sequential circuits. This paperisorganized as follows. Section II discusses the convert-coded-collect space theory and itsdefinitions. Section III

presents details about validation the quaternary based on the CCCitheory. Section IV shows how wecanimplement the two popular logic circuit both the combinational and sequential circuits. In section V wepresent design for two inputs MVL FPGA based on our new theory. Finally, section VI concludes the paper.

II. THE CONVERT-CODED-COLLECT SPACE THEORY

The proposed theory starting point is to expand binary logic to general MVL. The new general case called Convert-Coded-Collectspace. The first phase has converted phase has two functions: the first is to convert any input value to other possible values, while the second one is the rejection any input. The second phase is Coded phase that able to code any two input data to give a single output. The third phase is the Collect phase that use to collect each output of the second phase. This phase uses generally the maximum relation. The three phases have different relations in a closed set of values. The combinations of the three phases are called Convert-Coded-Collect (CCC). This section illustrates the mean of the CCC ispace and its operations.

Theorem

The Convert-Coded-Collect (CCCi) spaceisanyclosedspace has i integer values set S_i={0, 1, 2,…., i-1}. This space has three phases Convert, Coded, and Collect;itis able to containment logical functions the use to convert any input in the closed set S_i to any output in the same set Siunder the logical conditions. The Convert, Coded and Collect phases can be defined as follows:

Definition 1

Convert Phase has one input and one output, this phase able to convert any input A belong to $S_i$under the logical conditions to any other values in Si and convert any maximum value to the minimum value in Si. This phase required at least to $2\log_2(i)$ functions.

Définition 2

Coded phase has two inputs and multi-outputs, in this phase each acceptable combination for the two inputs A, B belong to S_i must be coded under the logical conditions to a unique value in S_i. Hence, an acceptable set to satisfy the conditions for this phase isE_i and $F_i$gates that define as in equations (1) and (2). This phase required at least to 2i functions.

$$E_i(A,B) = \begin{cases} max & If\ A = B = 1 \\ min & otherwise \end{cases} \quad (1)$$

$$F_i(A,B) = \begin{cases} B & If\ A = i \\ min & otherwise \end{cases} \quad (2)$$

Definition 3

Collect phase has multiple inputs and one output. In this phase the n inputs A, B, C, D belong to S_i will be generated under the logical conditions a single value in S_i. Hence, an acceptable function to satisfy the conditions for this phase is MAX (maximum) thatdefine as in equation (3). Also, it can MIN (minimum) or DIF (maximum-minimum). Another important gate supplemented with this phase is X gate that is an exchange switch and it is defined as in equation (4). This phase requiresat least to two functions. The CCCi space has at least to $2(i+1) + 2\log_2(i)$ functions:

$$MAX(A,B) = maximum(A,B) \tag{3}$$

$$XF_i(A,B)=Fi(B,A) \tag{4}$$

The following sub sectionis an example for the quaternary MVL, where i = 4 and the three phases are explained based on CCCi s pace theory.

III. QUATERNARY (CCC4) SPACE

The definition of CCCispace in the previous section requires to enhancement. The application of CCCi with the values S_4 = {0, 1, 2,3} (quaternary) iscalled CCC4. It enhances the solutions and the applications of the CCCi space. The three phases of CCC4 discuss as follows:

- **Convert Phase**

This phase has four main gates: LN, UN, LR, and UR. Thesegates able to present all the requirements of the convert phase in CCC4, and the additional gate (AN) isauxiliary function because it replace by LN and UN serially. AN will be neglected to reduce the number of gates. So, it can be defined lsimply as shown in Table 1.

Table 1: Truth Table for Convert Phase

Input	LN	UN	AN	LR	UR
0	1	2	3	0	0
1	0	3	2	0	1
2	3	0	1	2	0
3	2	1	0	2	1

- **Coded Phase**

The coded phase output in CCC4 space can be calculated based on equations (2) and (3) and the results are shown in Table 2.

Table 2: Truth Table for CCC4 Coded Phase

Inputs		Output							
A	B	E_0	E_1	E_2	E_3	F_0	F_1	F_2	F_3
0	0	3	0	0	0	0	0	0	0
0	1	0	0	0	0	1	0	0	0
0	2	0	0	0	0	2	0	0	0
0	3	0	0	0	0	3	0	0	0
1	0	0	0	0	0	0	0	0	0
1	1	0	3	0	0	0	1	0	0
1	2	0	0	0	0	0	2	0	0
1	3	0	0	0	0	0	3	0	0
2	0	0	0	0	0	0	0	0	0
2	1	0	0	0	0	0	0	1	0
2	2	0	0	3	0	0	0	2	0
2	3	0	0	0	0	0	0	3	0
3	0	0	0	0	0	0	0	0	0
3	1	0	0	0	0	0	0	0	1
3	2	0	0	0	0	0	0	0	2
3	3	0	0	0	3	0	0	0	3

It’s clear that there are eight gates under S_4 set.

- **Collect Phase**

In this phase the multiple inputs are collected and there is one output. For this phase is MAX (maximum) that define as in equations (3) and (4).

IV. DESIGN EXAMPLES

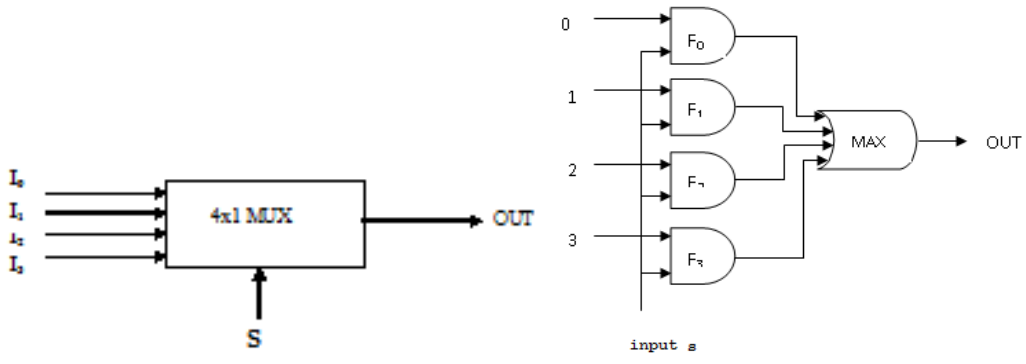
The arithmeti coperations and logical operationsat higher speed may be done using MVL. Implementation of digital system with these advantages achieved using VLSI and it has very simple electronic design implementation technique [8]. FPGA scontain programmable logic components called« logic blocks », and a hierarchy of reconfigurable interconnects that allow the blocks to be« wired together »some what like many (changeable) logicgates. It can be inter-wired in (many) different configurations. Logic blocks may be configured to perform complex combinational functions, or merely simple logicgates like AND and XOR. In mostFPGAs, the logic blocks alsoinclude memory elements, which may be simple flip-flops or more complete blocks of memory [9]. So, we enhance the new theory by designing the two types of digital circuits. These circuits, combinational and sequential, are the basic circuit implementation of the MVL FPGA unit. This section has two subsections ; the first shows the implementation of the MVL multiplexer in CCC4 space and the second gives the design of MVL D (Multistable) Flip-flop in CCC4 space.

- **Multiplexer in the CCC4 Space**

This section is an enhancement to the proof of the theory in the previous section. It selects a combinational logic circuit (Multiplexer) as an important circuit in the real world. The suggested introduces possibility to design a multiple-valued logic multiplexer based on the new theory. This approach may be demonstrated with designing the multiplié for any value of i in CCC is pace. An MVL multiplexer is a combinational circuit that selects one of the rn input lines based on a set of n selection lines and directs it to à single output line. Normally, there are rn inputs which come from a decoder and n select lines whose bit combinations determine which input to select. The design of 4x1 multiplexer (MUX) is presentedin Figure 1 and the operates is given in Table 3 [10].

Table 3: MVL Multiplexer Operation Table

S	OUT
0	I_0
1	I_1
2	I_2
3	I_3



(a) (b)

Figure 1: The Implementation of CCC4 MVL Multiplexer(a) Block Diagram, (b) MVL Logic Diagram

- **Flip-Flop in the CCC4 Space**

This section offes another enhancement to the proof of the theory in the previous section. Selecting a sequential logic circuit (Flip-Flop) as an important part in the digital systems. It shows that we can design a multiple-valued logic Flip-Flop based on the new theory and this approach may be used to design the Flip-Flop for any value of i in CCC is pace. Multiple-Valued Flip-Flops (MVLFF) are circuits that have more than two stable states (two state in binaryl ogic) and can be used to store state information. Output of flip-flop circuits depend on their input(s) with some equation. In multiple-valued logic, input-output equations are complicated. Operation of the D-type multiple-valued flip-flop issame as the binary case. Where the input is applied directly to S input and its complementis applied to the R input to eliminate the undesired condition in the binary RS flip-flop. The next – state equation is given by:

$$Qn+1=D \quad (5)$$

Where D is the flip-flop input and itisvalid for the binary case too [11],[12]. The gate implementation of D Multi-stable Flip-flop based on CCC is pace is given in Figure (2)

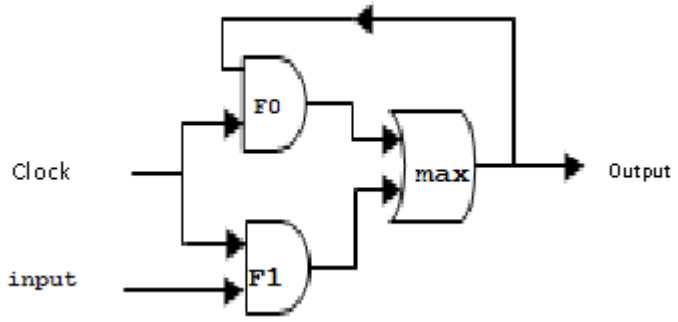


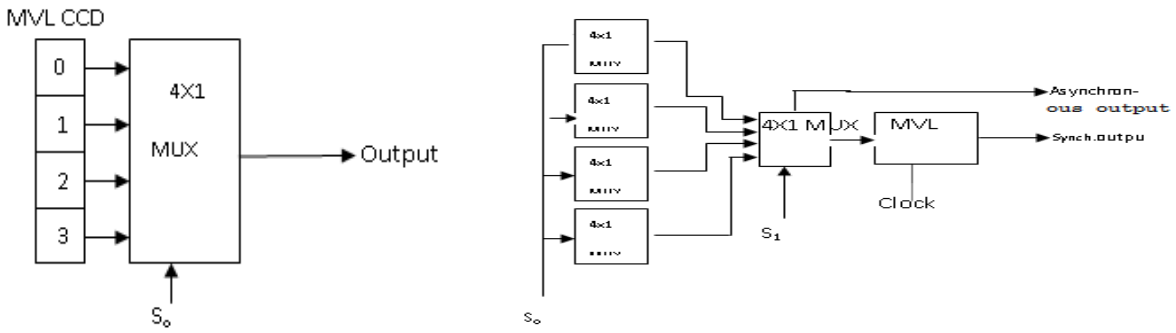
Figure 2: D-FF Based on CCC4 Space

V. IMPLEMENTATION OF TWO INPUT FPGA BASED ON CCC4

FPGA is an integrated circuit designed to be configured by a customer or a designer after manufacturing hence "field-programmable". Contemporary FPGAs have large resources of logic gates and RAM blocks to implement complex digital computations. As FPGA designs employ very fastIOs and bidirectional data buses it becomes a challenge to verify correct timing of valid data with in setup time and hold time. Floor planning enables resources allocation within FPGA to meet these time constraints. FPGA scanbe used to implementany logical function that an ASIC could perform. Also, the low non-recurring engineering costs relative to an ASIC design (not with standing the generally higher unit cost), offer advantages for many applications.[13]

The most basic building block of an FPGA is the Cell, or Slice. Typically, a slice has a few inputs, a Lookup Table (or LUT) which can be programmed to evaluate any Boolean function over those inputs, and one or more outputs, each of which can be configured to either update immediately when the input updates (asynchronous) or update only on the next clock tick, using a flip-flop built into the slice (synchronous). Some FPGA cells have additional capabilities, such as adder simplemented in hardware, to save using LUTs for this purpose[14]. The proposed FPGA slice, will use charge-coupled device (CCD) is a device for the movement of electrical charge, usually from within the device to an area where the charge can be manipulated, the CCD [15] is connected directly to the four MVL Multiplexers that implemented based on CCC4 (see F.g.3a), the combined outputs of the multiplexers are connected to another multiplexer.

The next component is the flip-flops, and the logic for selecting asynchronous or synchronous mode. The over all proposed two inputs MVL FPGA based on the CCC is pacet heory isgiven in Figure.3b.



(a) **(b)**

Figure 3: Two Input MVL FPGA Based on CCC4 Space (a) 4x1 MVL Multiplexer Unit Based on CCC4 Space (b) Block Diagram for the Proposed Two Inputs FPGA

VI. CONCLUSIONS

Increasing data processing capability per unit chip area and reducing the number of required computation steps can be achieved using MVL. The number of digits required in a MVL family is logi times less than that required in binary logic. This paper presents a new MVL theory called Convert-Coded-Collect (CCCi) space by extending the binarylogic theory as operations in a new space called Convert-Coded-Collect space (CCCi). An enhancement to the new theory is presented by designing the two popular types of digital circuits, both the combinational and sequential circuits are the basic circuit implementation of the MVL FPGA unit. The results show that the implementation of the MVL multiplexer in CCC4 space and the design of MVL D (Multistable) Flip-flop in CCC4 space are helpful because it has simple functions with a package of advantages. Finally, we trying to build a basic MVL FPGA unit based on the new theory and the designed multiplexer and flip-flops.

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